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10/763,889	01/23/2004	Tianlong Chen	3073.006A	6019

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EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,889	CHEN ET AL.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/11/05 - 6/22/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 24 is objected to because of the following informalities: the work "wherein" is repeated in line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 24, 27, 29, and 34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There appears to be support in the specification for providing a one-to-one ownership correspondence of a memory block to a computing device. Examiner asks the applicant to cite such supporting disclosure to overcome this rejection.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 35, 48, and 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The term "substantial computing time" in claim 35 is a relative term which renders the claim indefinite. The term "substantial computing time" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

7. Claim 48 recites the limitation "said other computing device" in line 3. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 51 recites the limitation "a network attached memory according to claim 50" in line 1. There is insufficient antecedent basis for this limitation in the claim. Is this referring to the network attached memory device in claim 50?

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 18-23, 25-26, 28, 30-33, 35-36, 40-43, & 45-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Horan et al. (US Patent # 5,914,727).

11. With respect to claim 18, Horan et al. disclose:

a CPU, as shown by item 102 in figure 2;

a memory having at least one memory block, as shown in figures 4-5;

a connection to a network, as shown by item 122 in figure 2;

a memory management function managing said memory block in said memory, as shown in figure 7;

means for providing access to said memory block to a computing device attached elsewhere to said network, as shown in figures 2-3.

12. With respect to claim 19, Horan et al. disclose wherein said means for providing access provides said computing device access to said memory block by direct memory address, as taught in column 5, line 11.

13. With respect to claim 20, Horan et al. disclose wherein said means for providing access provides said computing device access to said memory by memory address translation between a memory address in said computing device and a memory address in said network attached memory device, as shown in figure 7.

14. With respect to claim 21, Horan et al. disclose wherein said memory address comprises a DMCE Virtual Address, by showing said memory comprising at least one block having a starting address (as shown in figure 9), assigning a device ID to said at least one device in said computer system (as shown in figure 22A); assigning a block ID to said at least one block of memory (as shown by the base address in figure 9; and assigning an offset ID to a memory unit stored in said at least one block of memory (as shown by the offset address in figure 9).

15. With respect to claim 22, Horan et al. disclose wherein said means for providing access comprises means for treating a memory block in said memory is an extended part of a system memory in said computing device, as taught in column 4, line 30.

16. With respect to claim 23, Horan et al. disclose wherein said memory management function comprises means for providing a memory block in said memory to said computing device for access and marking said memory block as used, as taught by the dirty bit in figure 13A.

17. With respect to claim 25, Horan et al. disclose wherein said memory management function comprises means for keeping a record of used memory blocks in said memory, as taught by the dirty bit in figure 13A.

18. With respect to claim 26, Horan et al. disclose wherein said memory management function comprises means for keeping a record of unused memory blocks in said memory, as taught by the dirty bit in figure 13A.

19. With respect to claim 28, Horan et al. disclose wherein said memory management function further comprises means for marking said memory block as unused when said computing device gees said memory block, as taught by the dirty bit in figure 13A.

20. With respect to claim 29, Horan et al. disclose wherein said memory management function provides said computing device with exclusive access to said memory block.

21. With respect to claim 30, Horan et al. disclose wherein said memory management function comprises means for copying data from said memory block to said computing device when said computing device requests said data by providing a memory address of said memory block, as shown in figure 7.

22. With respect to claim 31, Horan et al. disclose wherein said data comprises image data, as shown by the graphics data in figure 7.

23. With respect to claim 32, Horan et al. disclose wherein said memory management function further comprises means for copying data received from said computing device into a memory block in said memory corresponding to a memory address received from said computing device, as shown in figure 7.

24. With respect to claim 33, Horan et al. disclose wherein said memory management function further comprises means for allocating a second memory block in said memory to said computing device, a shown in figures 4-6.

25. With respect to claim 34, Horan et al. disclose wherein said memory management function further comprises means for freeing a memory block from said one-to-one correspondence with said computing device.

26. With respect to claim 35, Horan et al. disclose wherein said memory management function uses substantial computing time of said CPU, by showing the processor involved in the address remapping in figure 7.

27. With respect to claim 36, Horan et al. disclose wherein said CPU is primarily dedicated to said memory management function, by showing the processor involved in the address remapping in figure 7.

28. With respect to claim 40, Horan et al. disclose:

at least one network attached memory device having memory, as shown in figure 2;

means for linking said at least one network attached memory device to a memory area network, as shown in figure 2;

wherein said at least one network attached memory device provides to at least one computing device located elsewhere on said network access said memory through a network connection, as shown in figures 2-3.

29. With respect to claim 41, Horan et al. disclose wherein said means for linking comprises a network connection, as shown by item 122 in figure 2.

30. With respect to claim 42, Horan et al. disclose:

a first network attached memory device having first memory, as shown by the graphics memory in figures 2-3; and

a second network attached memory device having second memory, as shown by the physical memory in figures 2-3;

wherein said first network attached memory device and said second network attached memory device are linked into a memory area network, and said first and second network attached memory devices provide to a separate computing device access said first memory and said second memory through a network connection, as shown in figure 2-3.

31. With respect to claim 43, Horan et al. disclose a service dispatch function which dispatches memory requests from said separate computing device to said first or second network attached memory devices and responds to said separate computing devices based on responses from said first or second network attached memory devices, as shown by the core logic circuitry in figure 3 and the address remapping in figure 7.

32. With respect to claim 45, Horan et al. disclose wherein said service dispatch function resides on a dedicated device separate from first and second network attached memory devices,

as shown by the core logic circuitry separate from the graphics and physical memories in figures 2-3.

33. With respect to claim 46, Horan et al. disclose wherein said memory requests comprise allocating memory, as taught in the abstract.

34. With respect to claim 47, Horan et al. disclose wherein said memory requests comprise copying data from said separate computing device to at least one of said first and said second memory, as shown in figure 7.

35. With respect to claim 48, Horan et al. disclose wherein said memory requests comprise copying data from said first or second memory in said memory area network to said other computing device, as shown in figure 7.

36. With respect to claim 49, Horan et al. disclose wherein said memory requests comprise freeing memory blocks from at least one of said first and said second network attached memory devices, as taught in column 32, lines 8+.

37. With respect to claim 50, Horan et al. disclose a hard disk, wherein data stored in said memory block can be copied to said hard disk and data stored in said hard disk may be copied to said memory block, as shown in figure 2.

38. With respect to claim 51, Horan et al. disclose wherein said data comprises image data, as shown by the graphics data in figure 2.

39. With respect to claim 52, Horan et al. disclose:

a CPU, as shown by item 102 in figure 2;

a memory having at least one memory block, as shown in figures 4-5;

a connection to a network, as shown by item 122 in figure 2;

a memory management function managing said memory block in said memory, as shown in figure 7;

wherein said network attached memory device provides access to said memory block to a computing device attached elsewhere to said network, as shown in figures 2-3.

40. With respect to claim 53, Horan et al. disclose a hard disk, wherein data stored in said memory block can be copied to said hard disk and data stored in said hard disk may be copied to said memory block, as shown in figure 2.

Claim Rejections - 35 USC § 103

41. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

42. Claims 24, 27, 29, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al. and Stamm et al. (US Patent # 5,404,482).

43. With respect to claim 24, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose wherein said memory management function comprises means for providing one-to-one ownership of a memory block in said memory to said computing device.

44. With respect to claim 27, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose wherein said memory management function comprises means for

keeping a record of said one-to-one ownership between said computing device and said memory block.

45. With respect to claim 34, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose wherein said memory management function further comprises means for freeing a memory block from said one-to-one correspondence with said computing device.

46. Stamm et al. teach in column 2, lines 15+, of a cache coherency system wherein only one of the processors, or the shared memory, may own the block of memory at any given time, and this ownership is indicated by an ownership bit for each block in the shared memory and in each of the caches. Analogously, resetting this ownership bit frees the block from its only owner.

47. With respect to claim 29, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose wherein said memory management function provides said computing device with exclusive access to said memory block. Stamm et al. teach such in column 2, line 7.

48. It would have been obvious to one of ordinary skill in the art, having the teachings of Horan *et al.* and Stamm *et al.* before him at the time the invention was made, to modify the caching system taught by Horan *et al.*, to include only one owner of a block and provide exclusive access to the block, as with the caching system of Stamm *et al.*, in order to maintain coherency, as taught by Stamm *et al.*.

49. Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al. and Ulrich et al. (US Patent Publication # 2002/0156973).

50. With respect to claim 37, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose an Ethernet connection. Ulrich et al. disclose such in paragraph 131.

51. With respect to claims 38-39, Horan et al. disclose all other limitations, as discussed above, but fail to specifically disclose wherein said memory comprises a plurality of memory blocks having different sizes, and wherein a size of said memory block is configurable.

52. Ulrich et al. disclose in paragraph 423 of as allowing for the use of different block sizes within each block, and in paragraph 549 of dynamic block sizes.

53. It would have been obvious to one of ordinary skill in the art, having the teachings of Horan *et al.* and Ulrich *et al.* before him at the time the invention was made, to modify the cache translation system taught by Horan *et al.*, to include an Ethernet connection and different sized and dynamically sized blocks, as with the cache translation system of Ulrich *et al.*, to improve the ability to utilize available memory space, as taught by Ulrich *et al.*.

54. Claim 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al..

55. The difference between Horan *et al.* and the claims is the claims recite the service dispatch function residing on the first network attached memory device, while Horan et al. show the chip logic circuitry separate from the graphics and physical memories. However, this specific configuration does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter of engineering choice to one skilled in the art to incorporate the chip logic circuitry into one of the memory devices of Horan *et al.* in order to conserve chip space, speed processing times, or any of a

number of other engineering benefits. (Please see also MPEP 2144.04 as to why making elements integral would generally be merely a matter of obvious engineering choice.)

Conclusion

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
Primary Examiner
Art Unit 2186